MP6603

55V, Dual Full-Bridge Motor Driver with Internal Current Sense

DESCRIPTION

The MP6603 is a dual full-bridge motor driver with integrated low-on resistance ($R_{DS(ON)}$) MOSFETs.

High integration and a small QFN package make the MP6603 a cost-effective solution for brushed DC motor drivers and stepper motor drivers.

The MP6603 operates across an 8V to 55V input voltage (V_{IN}) range. It can deliver a motor current up to 5A peak per full bridge, depending on the ambient temperature and PCB layout.

The MP6603 has unique independent ground pins for each half-bridge. These pins make it possible to provide current measurements through the external shunt resistor.

Two configurable input modes are available for the MP6603: a pulse-width modulation (PWM) input interface and an indexer interface. The IN_SEL pin configures the input interface.

Internal safety and diagnostic features include over-current protection (OCP), short-circuit protection (SCP), under-voltage protection (UVP), and thermal shutdown.

The MP6603 is available in a QFN-25 (4mmx5mm) package.

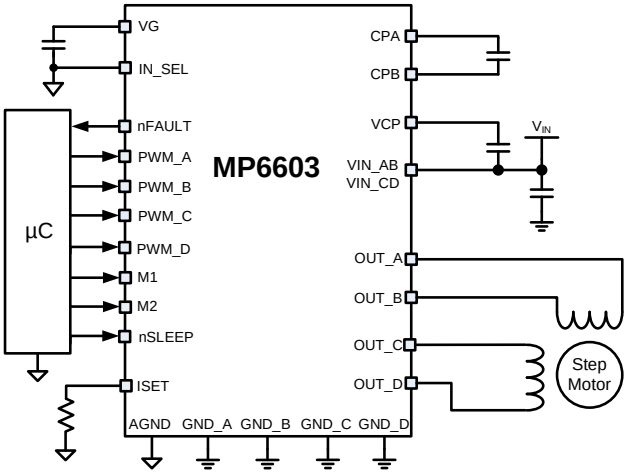
FEATURES

- Wide 8V to 55V Operating Input Voltage (V_{IN}) Range
- Two Internal Full-Bridge Drivers
- Selectable Input Interface: Simple Pulse-Width Modulation (PWM) Input or Indexer Input)
- Indexer Interface Offers Full-, Half-, Quarter-, and Eighth-Step Modes by Setting the M1 and M2 Pins
- Low On Resistance ($R_{DS(ON)}$): 65mΩ High-Side MOSFET (HS-FET) and 50mΩ Low-Side MOSFET (LS-FET)
- Up to 5A of Current in Full-Bridge Mode
- Up to 10A of Current in Parallel Mode
- PWM Operating Frequency Up to 100kHz
- Independent Ground Pins for Each Half-Bridge
- Over-Current Protection (OCP)
- Thermal Shutdown
- Under-Voltage Lockout (UVLO)
- Internal Charge Pump
- Fault Indication Output
- Available in a Space-Saving QFN-25 (4mmx5mm) Package

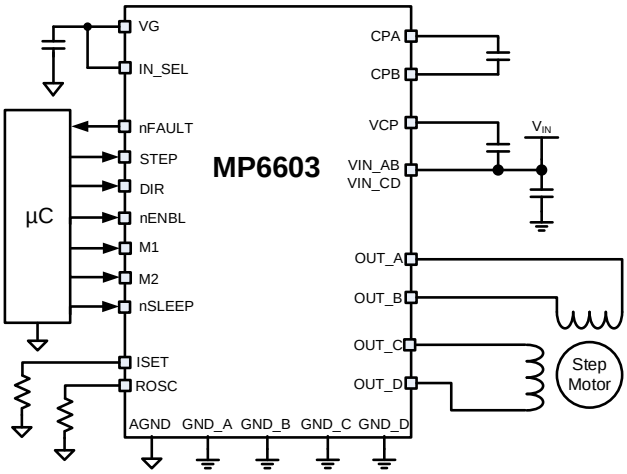
APPLICATIONS

- Bipolar Stepper Motors
- Brushed DC Motor Drivers

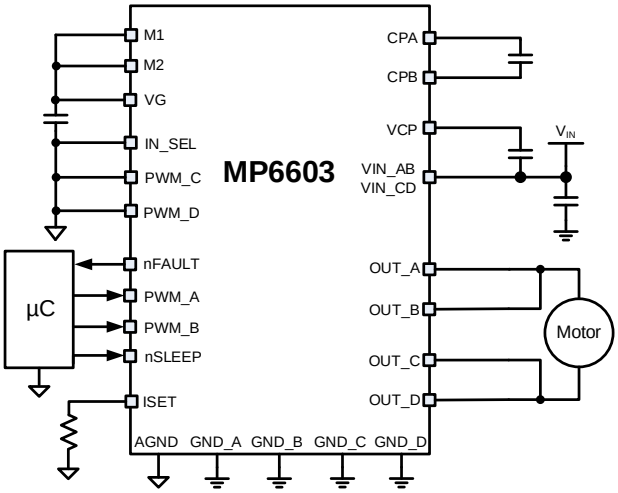
TYPICAL APPLICATION



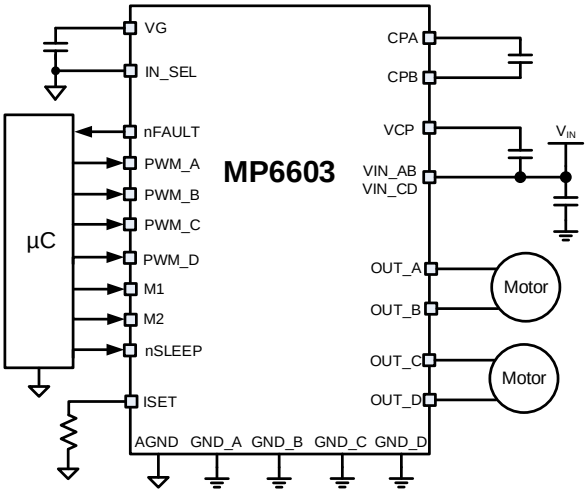
Stepper Motor Application with PWM Input



Stepper Motor Application with Indexer Input



Mono DC Motor Application with Parallel Mode



Dual DC Motor Application

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6603GV	QFN-25 (4mmx5mm)	*See Below*	1

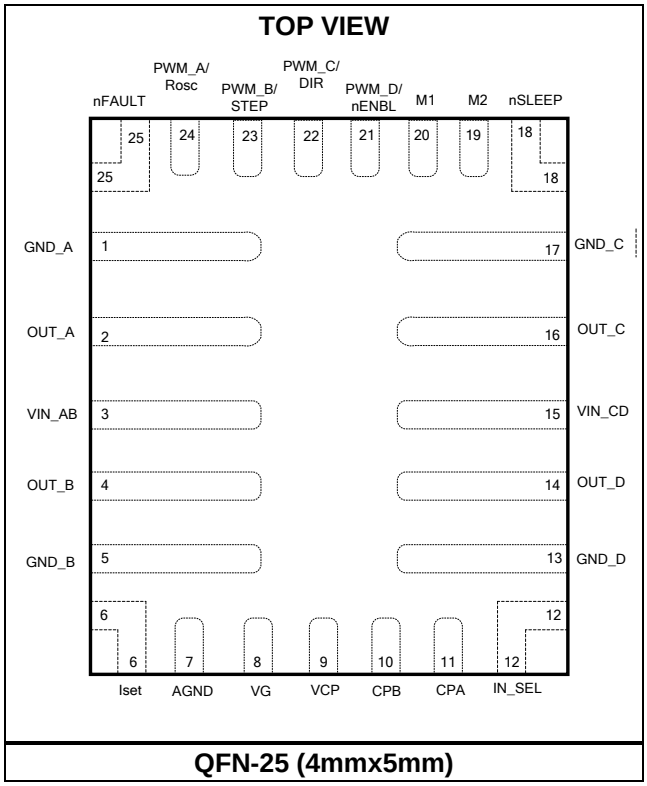
* For Tape & Reel, add suffix -Z (e.g. MP6603GV-Z).

TOP MARKING

MPSYWW
MP6603
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6603: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-25 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name		Description
1	GND_A		**Half-bridge A power ground.**
2	OUT_A		**Half-bridge A output terminal.**
3	VIN_AB		**Half-bridge A and B input supply voltage.** All VIN pins must be connected to the same supply. Decouple this pin to ground with a minimum 100nF ceramic capacitor for each VIN pin. In addition, a bulk capacitor with sufficient capacitance must be placed on the power supply pin.
4	OUT_B		**Half-bridge B output terminal.**
5	GND_B		**Half-bridge B power ground**
6	ISET		**Current set programming.** A resistor connected ISET to AGND sets the motor current.
7	AGND		**Signal ground.**
8	VG		**Low-side MOSFETs' (LS-FETs') gate drive voltage.** A 220nF, 16V ceramic capacitor must be placed between this pin and AGND.
9	VCP		**Charge pump output.** A 1µF, 16V ceramic capacitor must be placed between this pin and VIN.
10	CPB		**Charge pump capacitor terminals.** Connect a 100nF ceramic capacitor rated for the VIN voltage between these terminals.
11	CPA		
12	IN_SEL		**Input mode selection.** IN_SEL = 0 selects the PWM input interface, and IN_SEL = 1 selects the indexer interface.
13	GND_D		**Half-bridge D power ground.**
14	OUT_D		**Half-bridge D output terminal.**
15	VIN_CD		**Input supply voltage for half-bridge C and D.** All VIN pins must be connected to the same supply. Decouple this pin to ground with a minimum 100nF ceramic capacitor for each VIN pin. In addition, a bulk capacitor with sufficient capacitance must be placed on the power supply pin.
16	OUT_C		**Half-bridge C output terminal.**
17	GND_C		**Half-bridge C power ground.**
18	nSLEEP		**Sleep logic input.** Logic low for sleep mode and logic high to enable the device.
19	M2		**Mode selection pin 2.**
20	M1		**Mode selection pin 1.**
21	PWM_D		**Half-bridge D PWM input signal.** This pin function is enabled if IN_SEL = 0.
		nENBL	**Enable input.** This pin function is enabled if IN_SEL = 1. Pull this pin logic high to disable the bridge outputs and translator operation; pull it logic low to enable them. nENBL has an internal pull-down resistor.
22	PWM_C		**Half-bridge C PWM input signal.** This pin function is enabled if IN_SEL = 0.
		DIR	**Direction input.** This pin function is enabled if IN_SEL = 1. DIR has an internal pull-down resistor.
23	PWM_B		**Half-bridge B PWM input signal.** This pin function is enabled if IN_SEL = 0.
		STEP	**Step input.** This pin function is enabled if IN_SEL = 1. The rising edge sequences the translator and advances the motor one increment. STEP has an internal pull-down resistor.
24	PWM_A		**Half-bridge A PWM input signal.** This pin function is enabled if IN_SEL = 0.
		ROSC	**Constant-off-time (COT) configuration pin.** This pin function is enabled if IN_SEL = 1. A resistor connected between ROSC and ground sets the PWM off time.
25	nFAULT		**Fault indication.** This pin is an open-drain output, and is pulled logic low if a fault condition is recognized. An external pull-up resistor is required if this pin used.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +60V
V_{OUTx} .....-0.3V to V_{IN} + 0.3V
VCP, CPB .....V_{IN} to V_{IN} + 6.5V
GND_x to AGND.....-0.3V to +0.3V
All other pins to AGND.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
.....3.29W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....8V to 55V
GND_x to AGND.....-0.2V to +0.2V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-25 (4mmx5mm)	38	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on a JESD51-7, 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 40V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Input voltage (V_{IN}) operating range	V_{IN}		8		55	V
Turn-on threshold	V_{IN_ON}	V_{IN} rising edge		7	7.5	V
Turn-on hysteretic voltage	V_{IN_HY}			0.3		V
IC Supply						
Shutdown current	I_{IN_SD}	nSLEEP = 0			1	µA
Operating current		nSLEEP = 1, no switching		5.5	7	mA
		nSLEEP = 1, f_{PWMA} = f_{PWMB} = f_{PWMC} = f_{PWMD} = 20kHz		8	10	mA
Input Logic (PWMx, M1, M2, EN)						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Input high current	I_{IH}	V_{IN} = 5V	-20		+20	µA
Input low current	I_{IL}	V_{IN} = 0V	-20		+20	µA
Input pull-down resistance	R_{PD}			500		kΩ
Switching Frequency						
Externally applied pulse-width modulation (PWM) frequency	f_{PWM}				100	kHz
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 5V			1	µA
Power MOSFETs						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_A = 25°C		65	85	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_A = 25°C		50	65	mΩ
Body diode forward voltage	V_F	I_{OUT} = 1A			0.9	V
Minimum on time				400		ns
Propagation delay time (on)		PWMx high to OUTx on		200	350	ns
Propagation delay time (off)		PWMx low to OUTx off		190	250	ns
Output rise time		R_L = 50Ω, OUTx to GND		80	220	ns
Output fall time		R_L = 50Ω, OUTx to VIN		170	270	ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 40V, T_A = 25°C, unless otherwise noted.

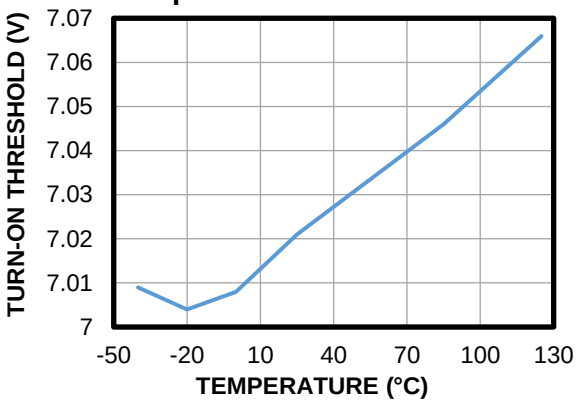
Parameters	Symbol	Condition	Min	Typ	Max	Units
Current Control						
Off time	t_{ITRIP}	After ITRIP, R_T = 100kΩ for indexer mode	20.5	23	24.5	µs
Peak current regulation level	I_{PEAK}	R_{ISET} = 39kΩ	3.8	4.0	4.2	A
ISET pin voltage	V_{ISET}		1.75	1.8	1.85	V
ISET pin current ratio	A_{ISET}	I_{ISET} / I_{OUT}	10.81	11.5	12.19	µA/A
Blanking time	t_{BLANK}			1000		ns
Current trip accuracy	ΔI_{TRIP}	R_{ISET} = 39kΩ, 71% to 100%	-5		+5	%
		R_{ISET} = 39kΩ, 38% to 67%	-10		+10	%
		R_{ISET} = 39kΩ, <34%	-15		+15	%
Protections						
Over-current (OC) threshold			7	9	11.5	A
Over-current protection (OCP) retry time	TOCR			2		ms
OC deglitch time (5)				500		ns
Input over-voltage protection (OVP) threshold	V_{OVP}		55.3	57.4	59.5	V
Input OVP hysteresis	ΔV_{OVP}			1000		mV
Thermal shutdown (5)				160		°C
Thermal shutdown hysteresis				35		°C
Charge pump frequency	f_{CP}		1800	2150	2600	kHz

Note:

5) Guaranteed by design.

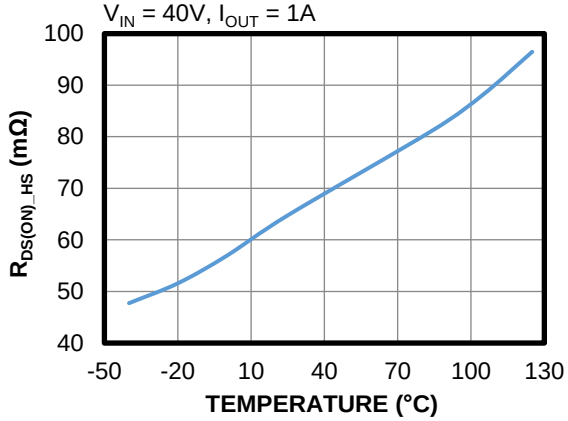
TYPICAL CHARACTERISTICS

V_{IN} Turn-On Threshold vs. Temperature



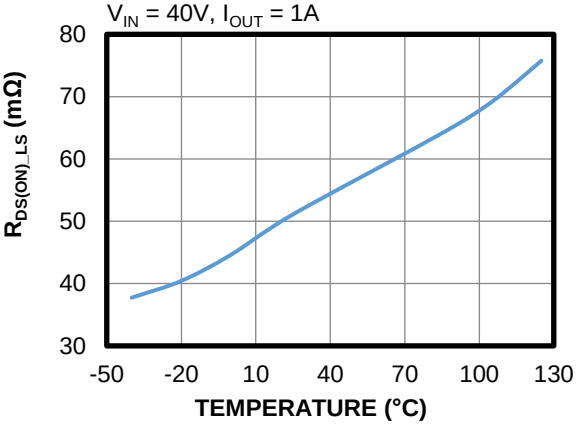
HS-FET On Resistance vs. Temperature

V_{IN} = 40V, I_{OUT} = 1A



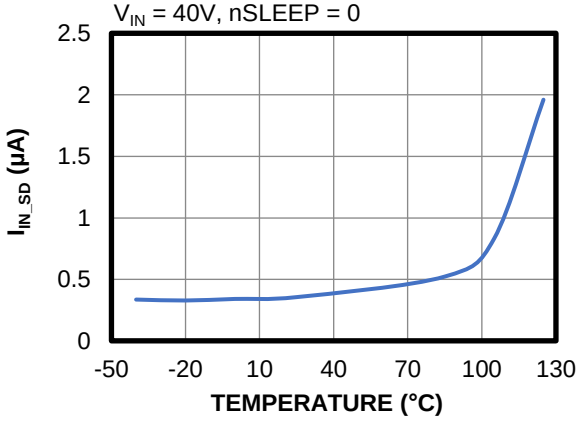
LS-FET On Resistance vs. Temperature

V_{IN} = 40V, I_{OUT} = 1A



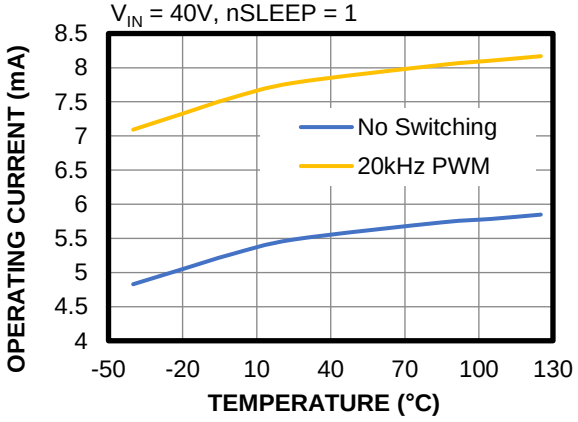
Shutdown Current vs. Temperature

V_{IN} = 40V, nSLEEP = 0



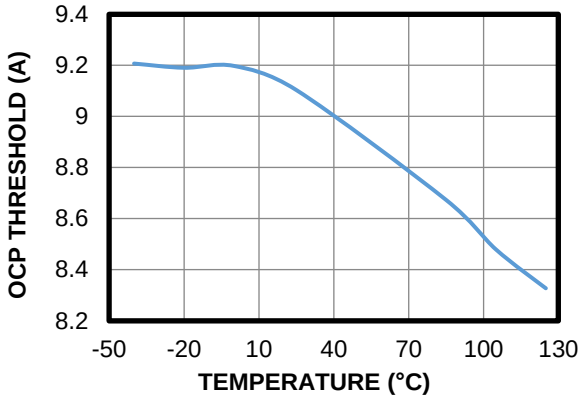
Operating Current vs. Temperature

V_{IN} = 40V, nSLEEP = 1



OCP Threshold vs. Temperature

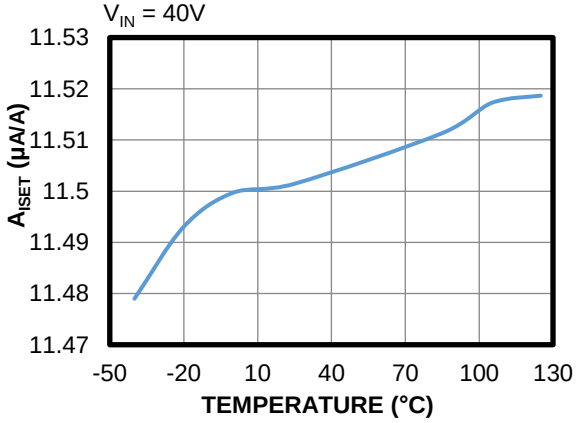
V_{IN} = 40V



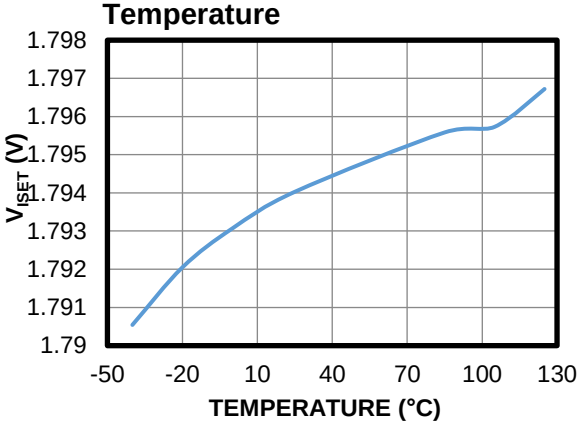
TYPICAL CHARACTERISTICS *(continued)*

ISET Pin Current Ratio vs. Temperature

V_{IN} = 40V



ISET Pin Voltage vs. Temperature

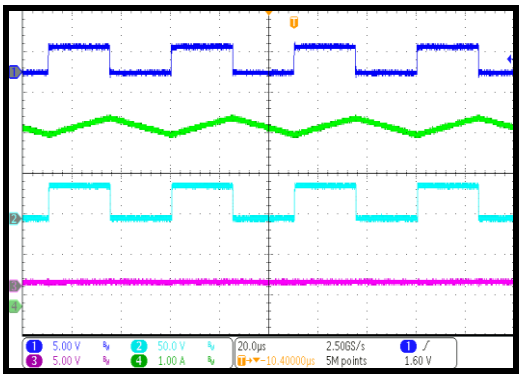


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 40V, nSLEEP = 3.3V, T_A = 25°C, load = resistor + inductor between OUTA and OUTB, OUTC and OUTD, unless otherwise noted.

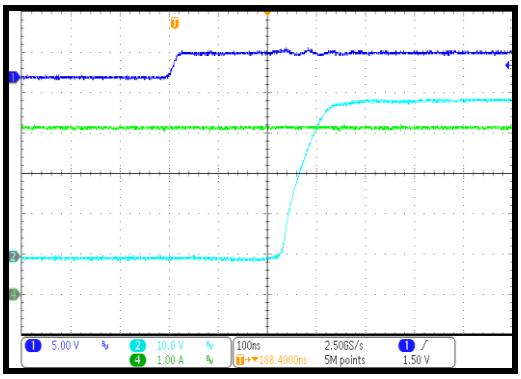
Steady State

IN_SEL = 0, M1 = 1,
M2 = 0 (4 half-bridges, PWM input)



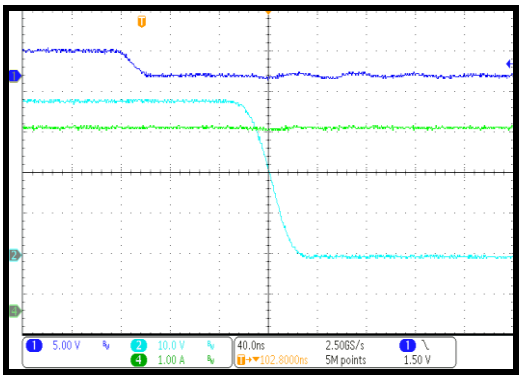
Steady State

IN_SEL = 0, M1 = 1,
M2 = 0 (PWMA to OUTA)



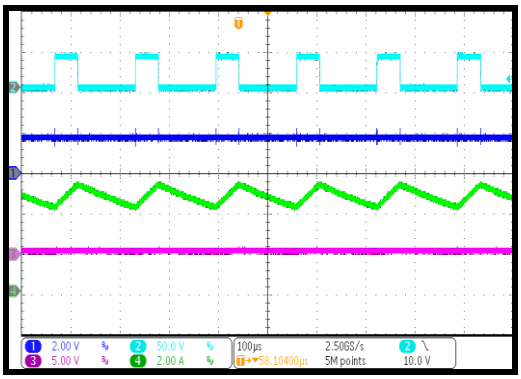
Steady State

IN_SEL = 0, M1 = 1, M2 = 0 (PWMA to OUTA)



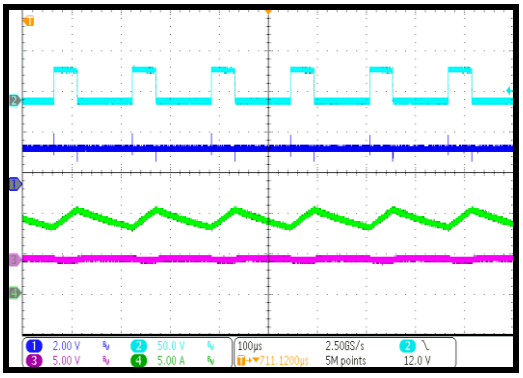
Steady State

IN_SEL = 0, M1 = 0,
M2 = 0 (4 half-bridges, current limit)



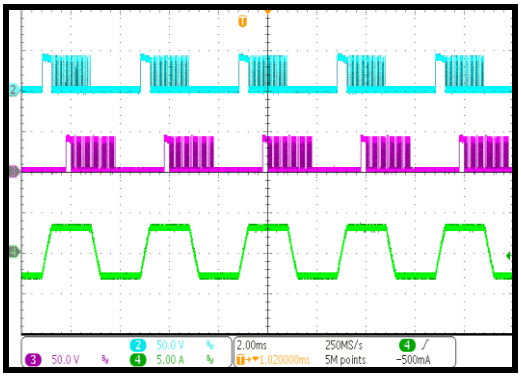
Steady State

IN_SEL = 0, M1 = 1,
M2 = 1 (parallel full-bridge)



Steady State

IN_SEL = 1, M1 = 0, M2 = 0 (full step)

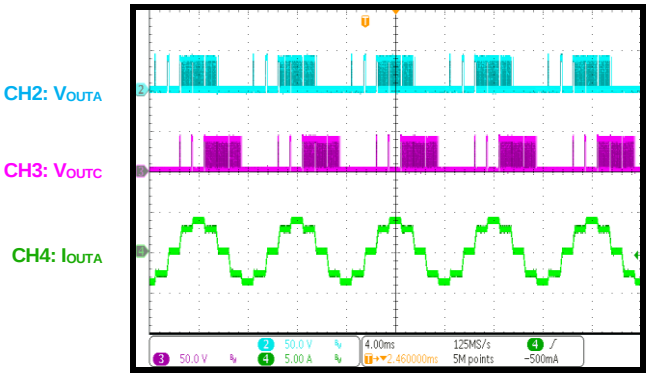


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 40V, nSLEEP = 3.3V, T_A = 25°C, load = resistor + inductor between OUTA and OUTB, OUTC and OUTD, unless otherwise noted.

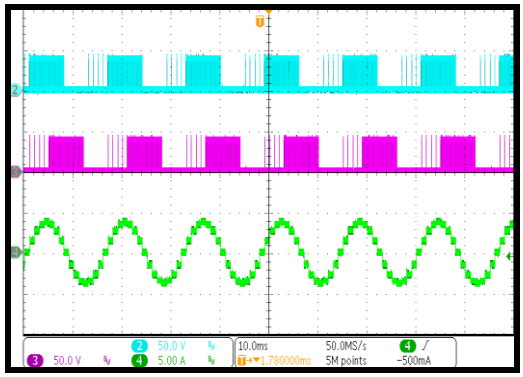
Steady State

IN_SEL = 1, M1 = 1, M2 = 0 (half-step)



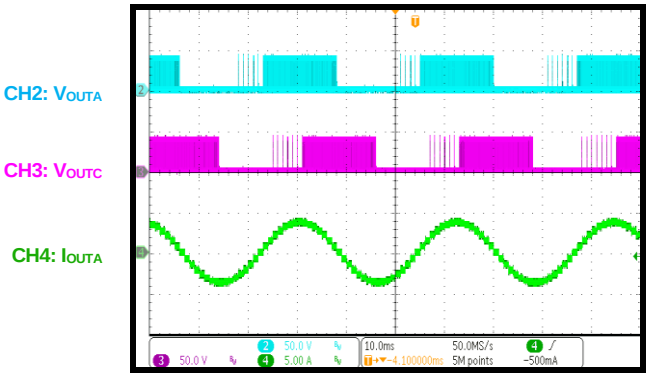
Steady State

IN_SEL = 1, M1 = 0, M2 = 1 (quarter-step)



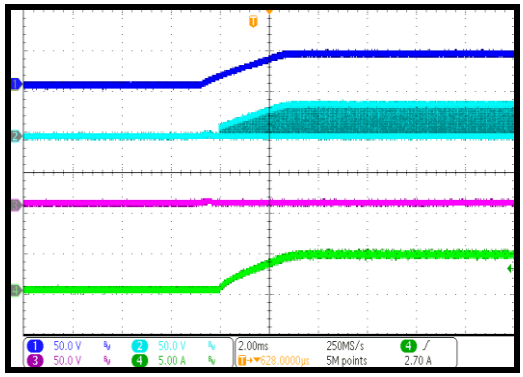
Steady State

IN_SEL = 1, M1 = 1, M2 = 1 (eighth-step)



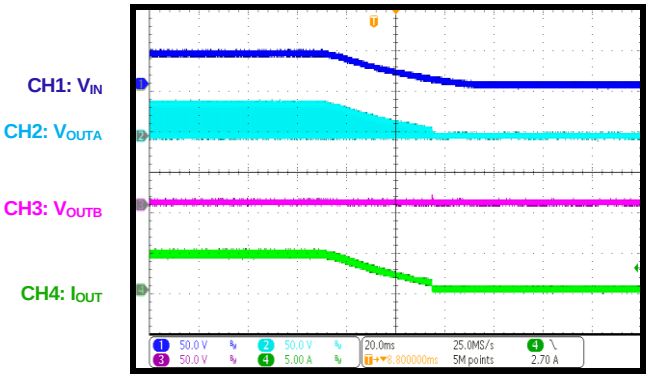
Power Ramping Up

IN_SEL = 0, M1 = 1,
M2 = 0 (4 half-bridges, PWM input)



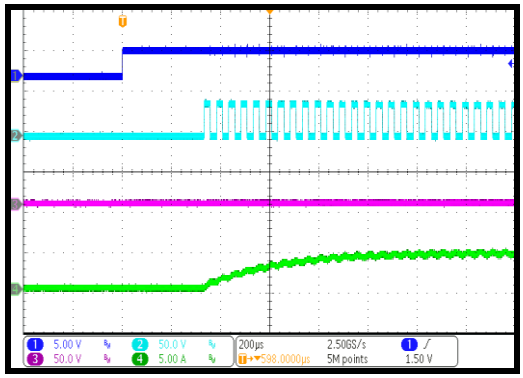
Power Ramping Down

IN_SEL = 0, M1 = 1,
M2 = 0 (4 half-bridges, PWM input)



nSLEEP Mode Recovery

IN_SEL = 0, M1 = 1,
M2 = 0 (4 half-bridges, PWM input)

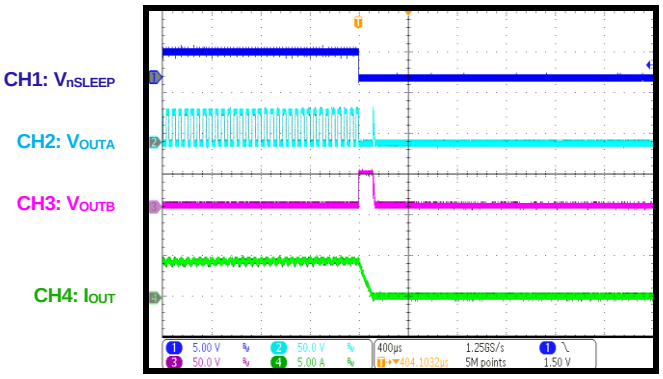


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 40V, nSLEEP = 3.3V, T_A = 25°C, load = resistor + inductor between OUTA and OUTB, OUTC and OUTD, unless otherwise noted.

nSLEEP Mode Entry

IN_SEL = 0, M1 = 1,
M2 = 0 (4 half-bridges, PWM input)



FUNCTIONAL BLOCK DIAGRAM

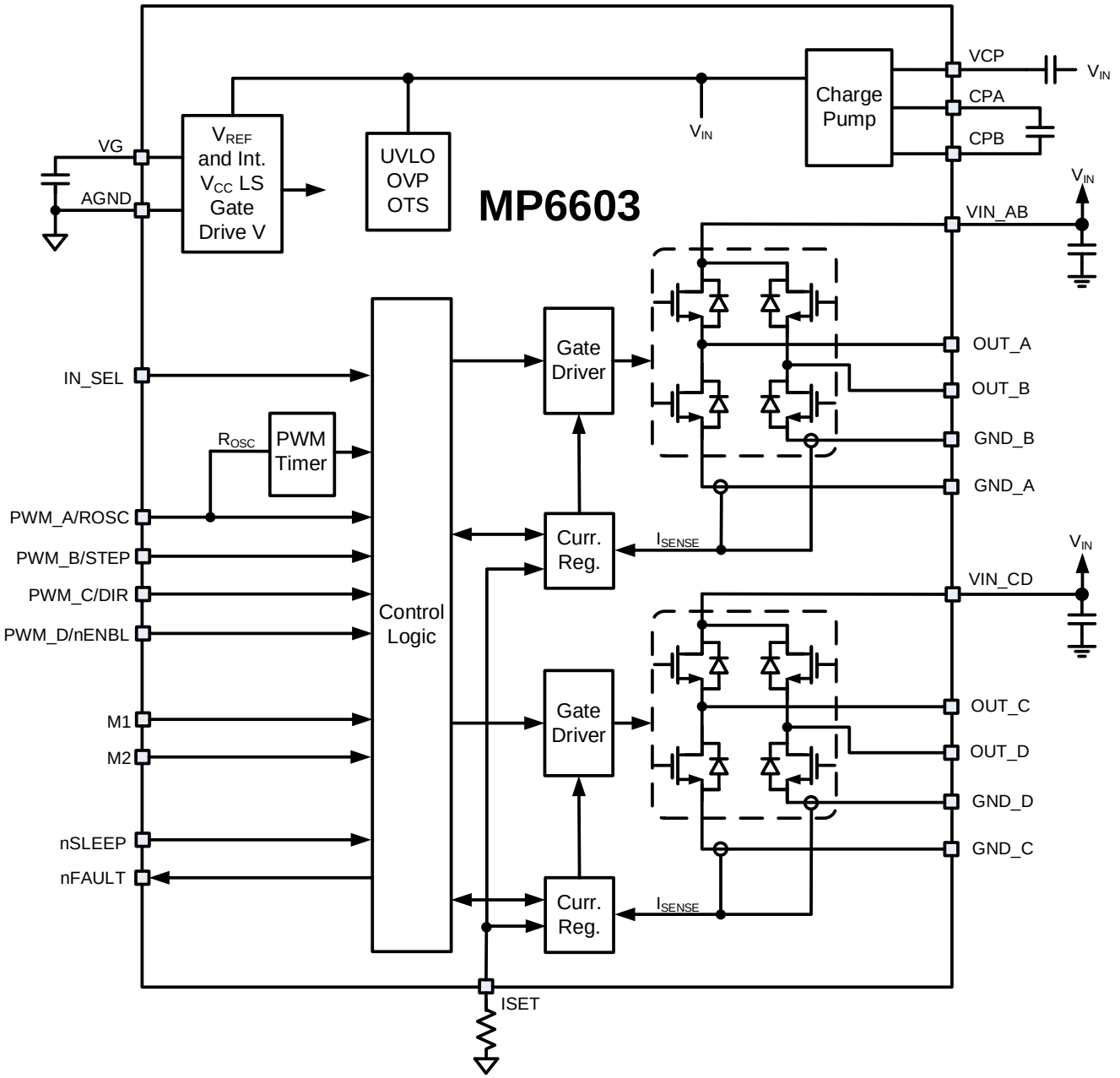


Figure 1: Functional Block Diagram

OPERATION

The MP6603 is a dual full-bridge motor driver with integrated low-on resistance ($R_{DS(ON)}$) MOSFETs. It can operate across a wide 8V to 55V input voltage (V_{IN}) range, and is designed to drive a stepper motor, two DC motors, or one high-current DC motor with two outputs in parallel.

The motor output current can be controlled either by an external pulse-width modulator or internal current regulation.

Input Logic

Two configurable input modes are available for the MP6603. The IN_SEL pin configures the input interface. IN_SEL = 0 selects the pulse-width modulation (PWM) input interface, and IN_SEL = 1 selects the indexer interface. Table 2, Table 3, and Table 4 show the logic truth tables for each input mode.

Pulse-Width Modulation (PWM) Input Control

The MP6603 supports a PWM input interface when IN_SEL = 0, and offers four different modes for different applications to drive bipolar stepper motors, brushed DC motors, or other loads (see Table 1). The motor current can be regulated by applying external PWM signals on the PWM_A, PWM_B, PWM_C, and PWM_D pins.

Table 1: Mode Selection for PWM Input Control

Mode	M2	M1	Outputs	Current Limit
1	0	0	4 half-bridges, OUT_x = PWM_x	Yes
2	0	1	4 half-bridges, OUT_x = PWM_x	No
3	1	0	2 full-bridges	Yes
4	1	1	Parallel full-bridge	Yes

For Modes 1 and 2, each half-bridge input PWM signal controls the corresponding half-bridge (i.e. OUTx = PWM_X).

In Mode 3, PWM_A and PWM_B control half-bridges A and B. PWM_C and PWM D control half-bridges C and D.

To relieve input/output (I/O) resources from the MCU, the PWM_B and PWM_D pins can be connected to GND, so that one PWM signal controls one full-bridge. In this set-up, PWM_A controls half-bridges A and B, and PWM_C controls half-bridges C and D). The operation of half-bridge B is complementary to half-bridge A, and the operation of half-bridge D is complementary to half-bridge C. Table 2 and Table 3 show the logic for Mode 3 (dual full-bridge).

Table 2: Input Logic Truth Table for OUT_A/B Mode 3

PWM_A (DIR)	PWM_B (nENBL)	OUT_A	OUT_B	Function (DC Motor)
H	L	H	L	Forward
L	L	L	H	Reverse
H	H	L	L	Brake
L	H	Z	Z	Coast

Table 3: Input Logic Truth Table for OUT_C/D Mode 3

PWM_C (DIR)	PWM_D (nENBL)	OUT_C	OUT_D	Function (DC Motor)
H	L	H	L	Forward
L	L	L	H	Reverse
H	H	L	L	Brake
L	H	Z	Z	Coast

Mode 4 is parallel full-bridge mode, in which PWM_A controls half-bridges A and B, and PWM_B controls half-bridges C and D. The PWM_C and PWM_D pins are the enable control pins. Bridges A and B are synchronized internally (even during cycle-by-cycle current limiting), as are bridges C and D. OUT_A and OUT_B should be connected together, and OUT_C and OUT_D should be connected together.

Table 4 and Table 5 on page 15 show the logic for Mode 4 (parallel full-bridge).

Table 4: Input Logic Truth Table for OUT_A/B Mode 4

PWMA (PWM for OUT_A/B)	PWMC (nEN for OUT_A/B)	OUT_A/B
H	L	H
L	L	L
x	H	Z

Table 5: Input Logic Truth Table for OUT_C/D Mode 4

PWMB (PWM for OUT_C/D)	PWMD (nEN for OUT_C/D)	OUT_C/D
H	L	H
L	L	L
x	H	Z

PWM Input Interface Current Limit

1. The current in the outputs is limited using constant-off-time (COT) PWM control circuitry. Operation is as follows: Initially, a diagonal pair of MOSFETs turns on and drives current through the load.
2. The load current (I_{LOAD}) increases, which is sensed by the internal current-sense (CS) circuit.
3. If I_{LOAD} reaches the current trip threshold (I_{TRIP}), the H-bridge switches to slow decay mode, and the two low-side MOSFETs (LS-FETs) turn on.
4. After a fixed off time (t_{ITRIP}), if I_{LOAD} falls ≥20% below the current limit threshold, the MOSFETs are re-enabled and the cycle repeats (see Figure 2).
5. If I_{LOAD} is still above I_{TRIP}, then t_{ITRIP} is extended until I_{LOAD} falls to 20% below the current limit threshold.

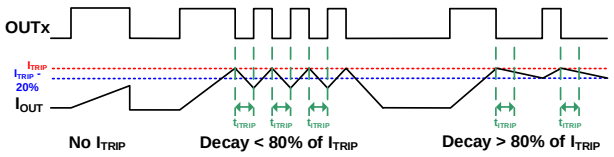


Figure 2: Current Regulation

I_{TRIP} can be calculated using Equation (1):

$$I_{TRIP} = 156k\Omega / R_{ISET} \quad (1)$$

Indexer Input

The MP6603 supports an indexer input interface when IN_SEL = 1, which is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. The currents in each of the two outputs are regulated with a configurable COT PWM control circuitry. The MP6603 integrates internal current-sensing; no external sense resistors are required.

Stepping

The motor moves step by step by applying a series of pulses to the STEP pin. A rising edge on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the digital-to-analog converters (DACs) and the direction of current flow in each winding. The increment amplitude is determined by the state of inputs M1 and M2 (see Table 2 and Table 3 on page 14).

The DIR pin's state determines the direction of the rotation of the stepper motor.

The nENBL pin controls the output drivers. When nENBL is low, the H-bridges' outputs are enabled, and the rising edges on the STEP pin are recognized. When nENBL is high, the H-bridges' outputs are disabled, and the STEP input is ignored. nENBL has an internal pull-down resistor.

The minimum STEP pulse width is 1µs. The Mx and DIR logic control inputs require a set-up time (t_C) of at least 200ns and a hold time (t_D) to the rising edge of the STEP input (see Figure 3 and Table 6).

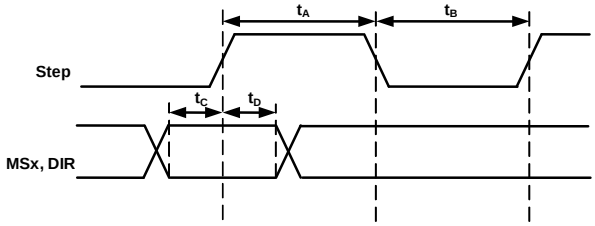


Figure 3: STEP Input Timing

Table 6: Logic Timing Specifications

Time Duration	Symbol	Typ	Units
Step minimum high pulse width	t_A	1	µs
Step minimum low pulse width	t_B	1	µs
Set-up time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Configurable Constant-Off-Time (COT) Current Control

The motor current is regulated by a configurable, COT PWM current control circuit. Its operation is described below:

1. Initially, a diagonal pair of MOSFETs turns on and drives current through the motor winding.

2. The current increases in the motor winding, which is sensed by an internal CS circuit. During the initial blanking time (t_{BLANK}), the high-side MOSFET (HS-FET) always turns on in spite of current limit detection.
3. When the current reaches I_{TRIP}, the internal current comparator either shuts off the HS-FET so the winding inductor current (I_L) freewheels through the two LS-FETs (slow decay) or turns on another diagonal pair of MOSFETs so that the current flows back to the input (fast decay).
4. The current keeps decreasing for the COT period (t_{OFF}) unless a zero-current level is detected (ZCD). After that, the HS-FET is enabled to increase the winding current again.
5. The cycle then repeats.

t_{OFF} is determined by the selection of an external resistor (R_T), which can be estimated with Equation (2):

$$t_{OFF}(ns) = 190 \times R_T(k\Omega) \quad (2)$$

The full-scale (100%) regulation current (I_{MAX}) can be calculated using Equation (3):

$$I_{MAX} = 156k\Omega / R_{ISET} \quad (3)$$

The DAC output reduces the trip current (I_{TRIP}) in precise steps. I_{TRIP} can be calculated with Equation (4):

$$I_{TRIP} = \%\ of\ I_{TRIP} \times I_{MAX} \quad (4)$$

See Table 8 on page 18 for the % of I_{TRIP} at each step.

Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously shutting down the HS-FET.

After the PWM cycle begins, the CS comparator's output is ignored for the fixed blanking time. This blanking time results in a minimum on time (t_{ON_MIN}) for the PWM cycle.

Automatic Decay Mode

The MP6603 uses a fully automatic decay mode to provide accurate current regulation.

Initially, slow decay is used. At the end of the fixed off time, if the current is above the I_{TRIP} threshold, then fast decay mode is initiated (by reversing the state of the H-bridges' outputs).

As soon as the current level during this fast decay period drops below the I_{TRIP} threshold, slow decay is again engaged for another fixed off time. After the completion of this second fixed off time, a new PWM cycle begins.

Figure 4 shows automatic decay mode operation during a current reduction as a result of a step input.

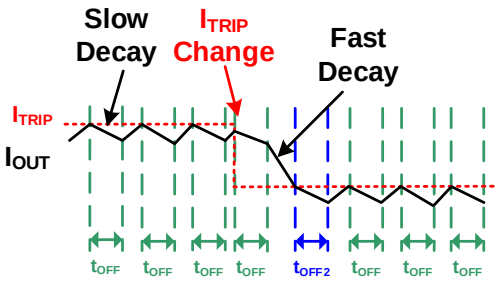


Figure 4: Slow Decay during t_{OFF} Unless I_{OUT} > I_{TRIP} at the End of t_{OFF}

In some cases, such as high voltage and low inductance, or regulation of very small currents, the PWM cycle's t_{ON_MIN} (set by the blanking time described above) can cause the current to rise very quickly. In this case, both slow and fast decay are used (see Figure 5).

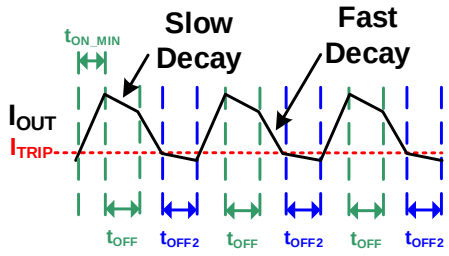


Figure 5: Current Regulation for Low Current and Low Inductance

Microstep Selection (M1 and M2)

When IN_SEL = 1, the MP6603 supports an indexer input interface, and the step mode is selected by applying logic high and low voltages to the M1 and M2 pins (see Table 7 on page 17). The MP6603 supports full-, half-,

quarter-, and eighth-step modes for progressively finer step resolution and control.

Table 7: Stepping Format

M2	M1	STEP MODE
0	0	Full Step
0	1	Half-Step
1	0	Quarter-Step
1	1	Eighth-Step

Full step includes four states, for which each motor winding is driven with either a 70.7% maximum positive current or a 70.7% maximum negative current.

This provides 4 steps per electrical rotation. Half-step creates 8 steps per electrical rotation. Quarter- and eighth-step provide 16 and 32 steps per rotation, respectively.

Table 8 on page 18 and Figure 6, Figure 7, Figure 8, and Figure 9 on pages 19–20 show the relative current level sequence for the different Mx settings. At each rising edge of the STEP input, the indexer transitions to the next state in the table. The direction is shown with the DIR pin high; the sequence is reversed if the DIR pin is low. The reset state is 45 degrees, which is entered at start-up or when waking up from sleep mode.

The Mx pins have internal pull-down resistors.

nSLEEP Operation

Driving nSLEEP low forces the device into a low-power sleep state. In this state, the gate drive charge pump is stopped, and all the internal circuits and H-bridges' outputs are disabled. All inputs are ignored when nSLEEP is low.

When waking up from sleep mode, there is a delay (about 500μs) before normal operation begins, which allows the internal circuitry to stabilize. The nSLEEP pin has an internal pull-down resistor.

Fault

The MP6603 features an nFAULT pin, which detects and reports fault conditions, such as over-current protection (OCP), over-temperature protection (OTP) and over-voltage protection (OVP). This pin is an open-drain output, and is driven low if a fault condition occurs. Once the fault condition is released, the nFAULT pin is pulled high by an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry limits the current through the MOSFETs by disabling the gate driver. If the over-current (OC) limit threshold is reached and lasts for longer than the OC deglitch time, all MOSFETs in the H-bridges are disabled and the nFAULT pin is driven low. The driver remains disabled for 2ms (typical), at which time it is automatically re-enabled.

OC conditions on both high-side (HS) and low-side (LS) devices (e.g. a short to ground, supply, or across the motor winding) all result in an OC shutdown. Note that OCP does not use the CS circuitry used for PWM current control.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the OVP threshold, the H-bridges' outputs are disabled and the nFAULT pin is driven low. Once V_{IN} drops to within its normal operation range, this protection is released and the device resumes normal operation.

Input UVLO Protection

If at any time V_{IN} falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled and internal logic is reset. Once V_{IN} exceeds the UVLO threshold, the device resumes normal operation.

Thermal Shutdown

If the die temperature exceeds safe limits, all MOSFETs in the H-bridges are disabled and the nFAULT pin is driven low. Once the die temperature returns to a safe level, the device automatically resumes normal operation.

Table 8: Relative Current Level Sequence (DIR = 1)

Eighth-Step #	Quarter-Step #	Half-Step #	Full Step #	Phase A Current, % of I_{TRIP_LIMIT} (%)	Phase B Current, % of I_{TRIP_LIMIT} (%)	Step Angle (°)
1	1	1	-	100.00	0.00	0.0
2	-	-	-	98.08	19.51	11.3
3	2	-	-	92.39	38.27	22.5
4	-	-	-	83.15	55.56	33.8
5	3	2	1	70.71	70.71	45.0 (reset state)
6	-	-	-	55.56	83.15	56.3
7	4	-	-	38.27	92.39	67.5
8	-	-	-	19.51	98.08	78.8
9	5	3	-	0.00	100.00	90.0
10	-	-	-	-19.51	+98.08	+101.3
11	6	-	-	-38.27	+92.39	+112.5
12	-	-	-	-55.56	+83.15	+123.8
13	7	4	2	-70.71	+70.71	+135.0
14	-	-	-	-83.15	+55.56	+146.3
15	8	-	-	-92.39	+38.27	+157.5
16	-	-	-	-98.08	+19.51	+168.8
17	9	5	-	-100.00	0.00	+180.0
18	-	-	-	-98.08	-19.51	+191.3
19	10	-	-	-92.39	-38.27	+202.5
20	-	-	-	-83.15	-55.56	+213.8
21	11	6	3	-70.71	-70.71	+225.0
22	-	-	-	-55.56	-83.15	+236.3
23	12	-	-	-38.27	-92.39	+247.5
24	-	-	-	-19.51	-98.08	+258.8
25	13	7	-	0.00	-100.00	+270.0
26	-	-	-	+19.51	-98.08	+281.3
27	14	-	-	+38.27	-92.39	+292.5
28	-	-	-	+55.56	-83.15	+303.8
29	15	8	4	+70.71	-70.71	+315.0
30	-	-	-	+83.15	-55.56	+326.3
31	16	-	-	+92.39	-38.27	+337.5
32	-	-	-	+98.08	-19.51	+348.8

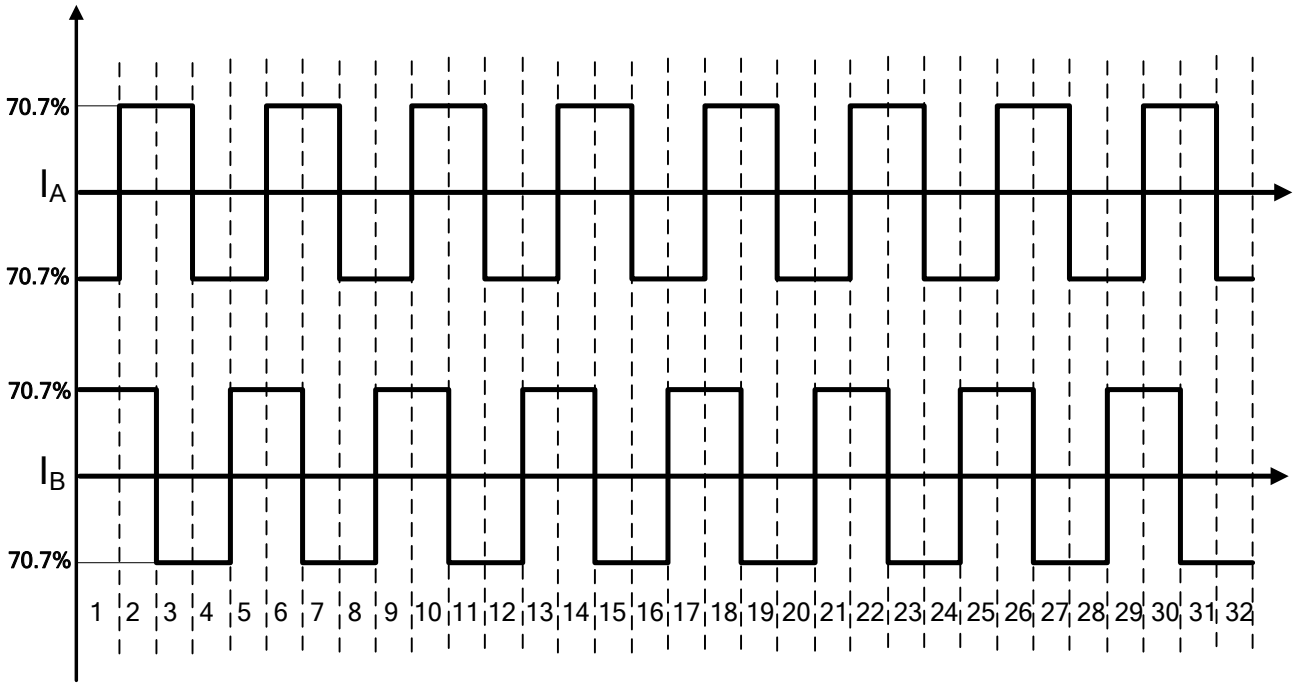


Figure 6: Full Step (4 Step Sequences)

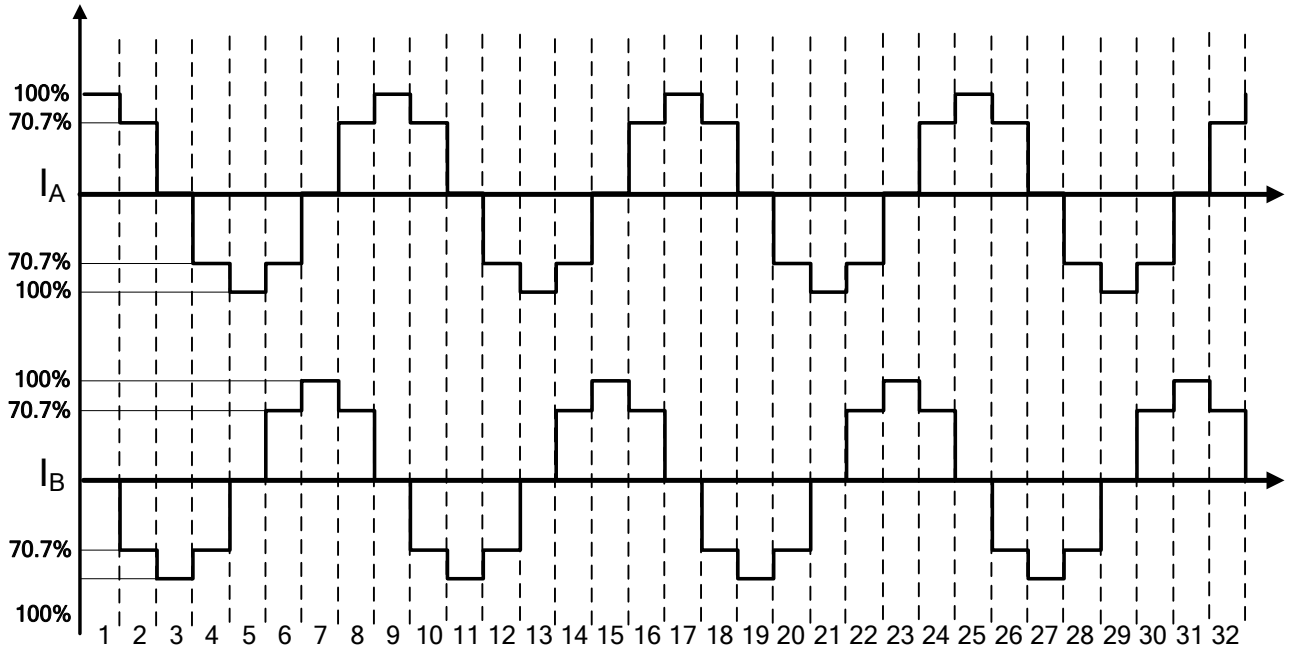


Figure 7: Half-Step (8 Step Sequences)

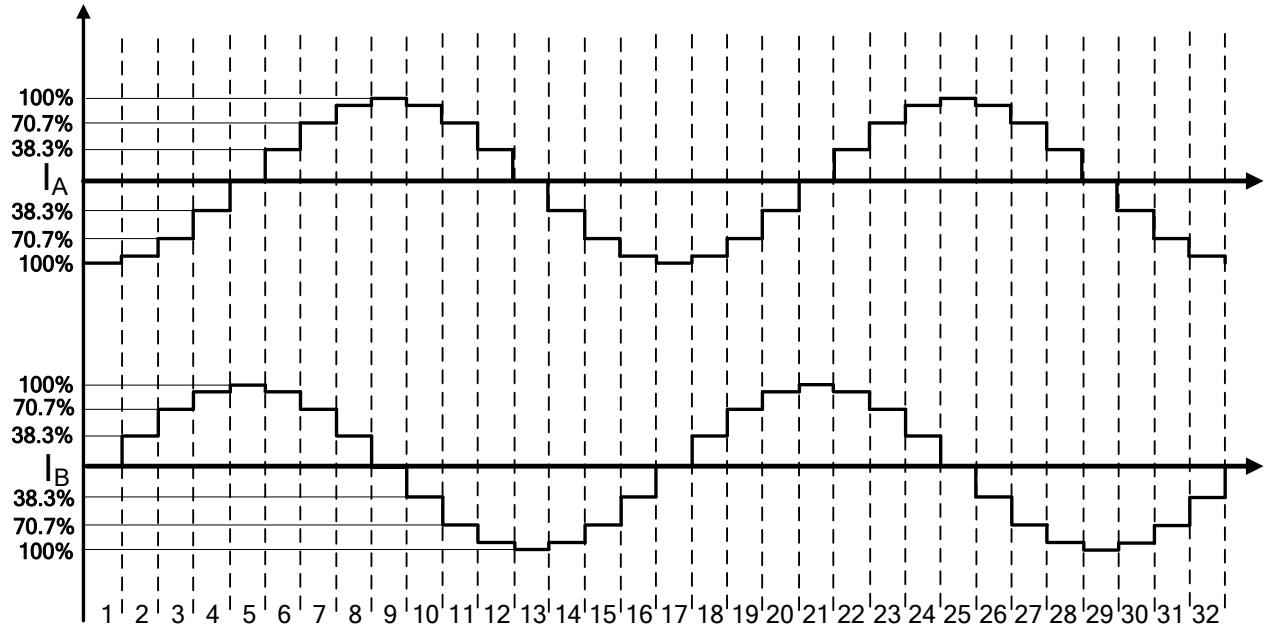


Figure 8: Quarter-Step (16 Step Sequences)

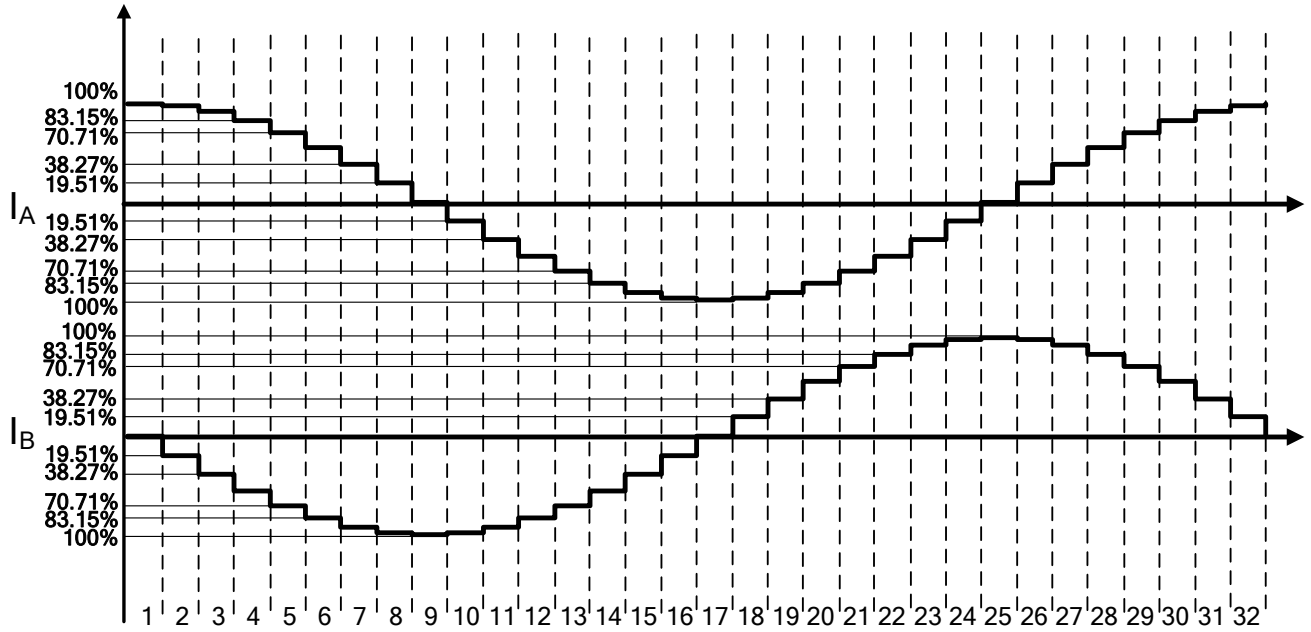


Figure 9: Eighth-Step (32 Step Sequences)

APPLICATION INFORMATION

External Shunt Resistor Selection Restrictions

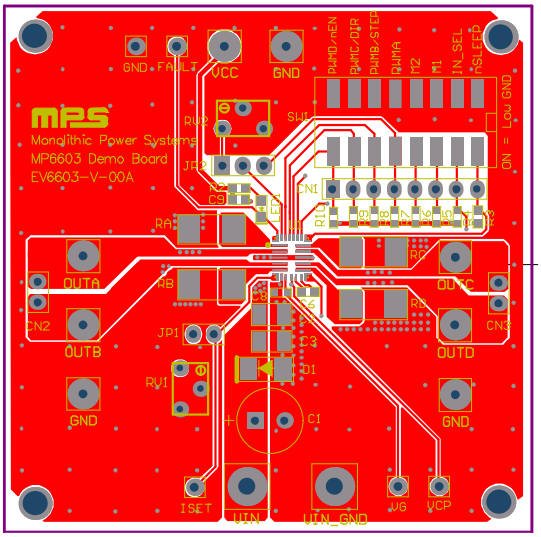
The MP6603 has unique independent ground pins for each half-bridge. These pins make it possible to provide current measurement through an external shunt resistor.

Care must be taken to ensure that the GND_x voltage is below 200mV. For example, for a 5A peak application, the external shunt resistors should be less than 40mΩ.

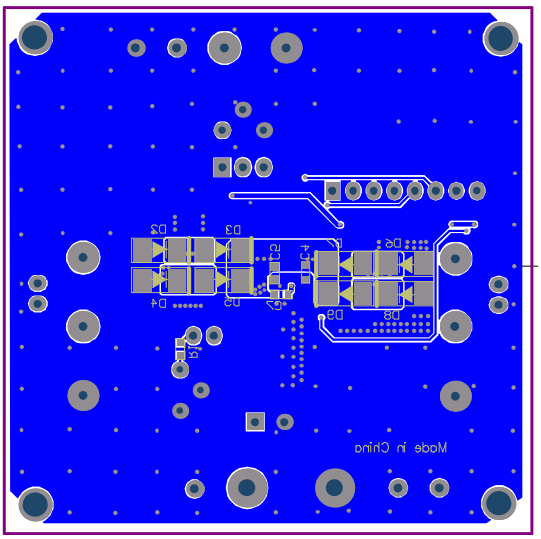
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 10 and follow the guidelines below:

1. Bypass the two VIN pins (VIN_AB and VIN_CD) to GNDx using a minimum 100nF ceramic capacitor with X7R dielectrics, placed as close to the IC as possible. Place an additional 1µF to 10µF ceramic capacitor close to the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize V_{IN}.
2. Connect a 100nF ceramic capacitor rated for V_{IN} between the CPA and CPB pins. Connect a 1µF, 16V ceramic capacitor between the VIN_AB, VIN_CD, and VCP pins.
3. Connect a 220nF, 16V ceramic capacitor with X7R dielectrics between the VG pin and AGND.
4. Place the supply bypass and charge pump capacitors as close as possible to the IC (ideally, adjacent to the IC pins on the same PCB layer).
5. Place as much copper as possible on the long pads.
6. Place large copper areas on the pads, and on the same outer copper layer as the device.
7. Solder the thermal pad directly to copper on the PCB.
8. Add thermal vias to transfer heat to the other layers of the PCB.



Top Layer



Bottom Layer

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

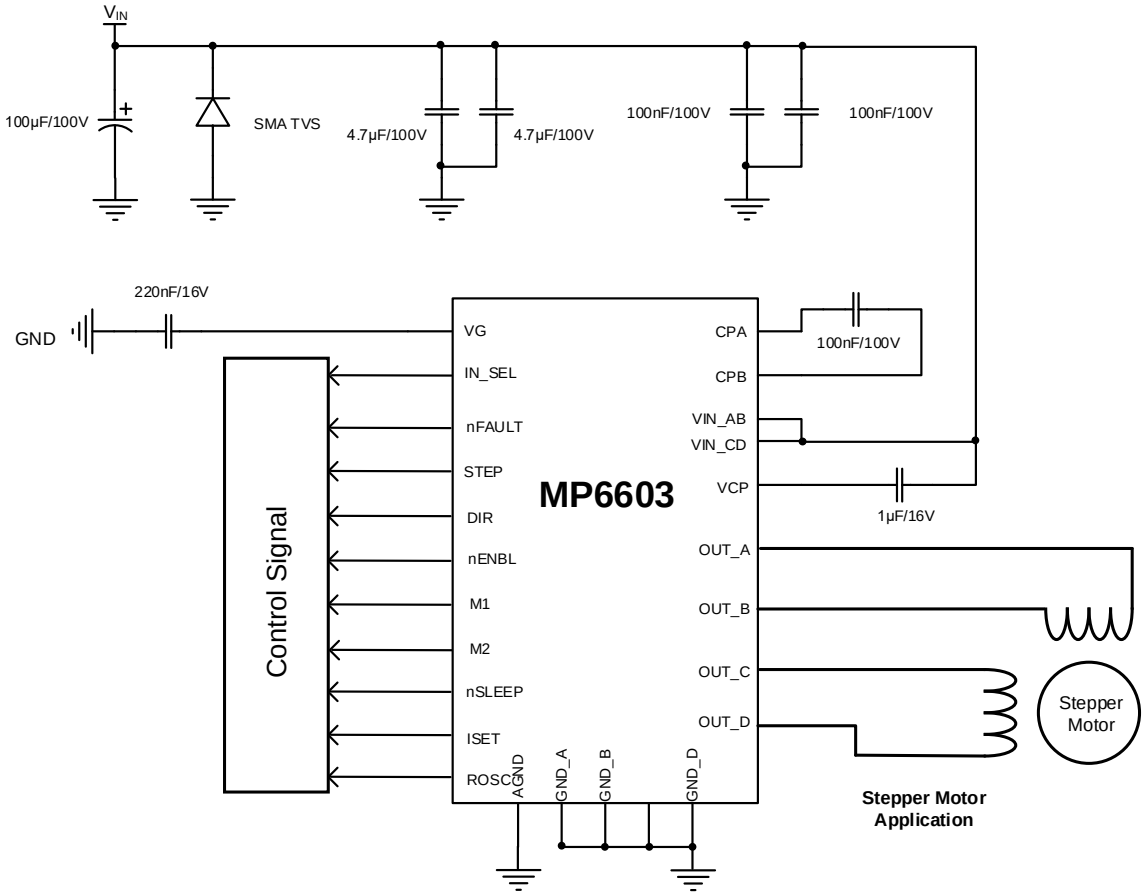
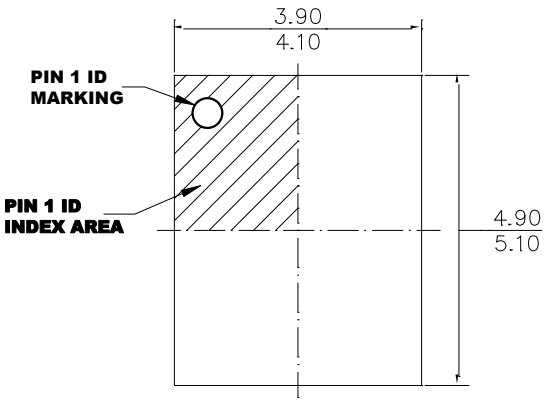


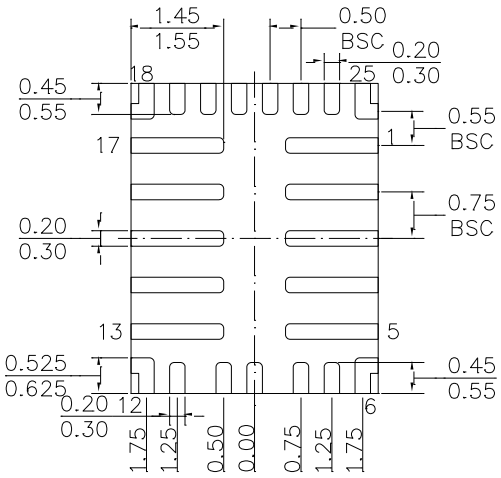
Figure 11: Typical Application Circuit

PACKAGE INFORMATION

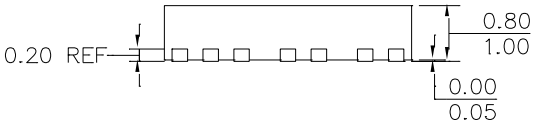
QFN-25 (4mmx5mm)



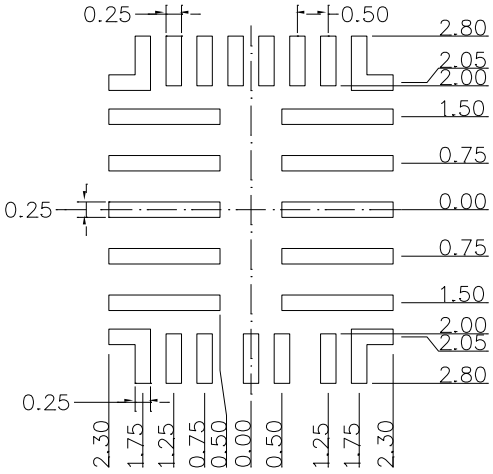
TOP VIEW



BOTTOM VIEW



SIDE VIEW

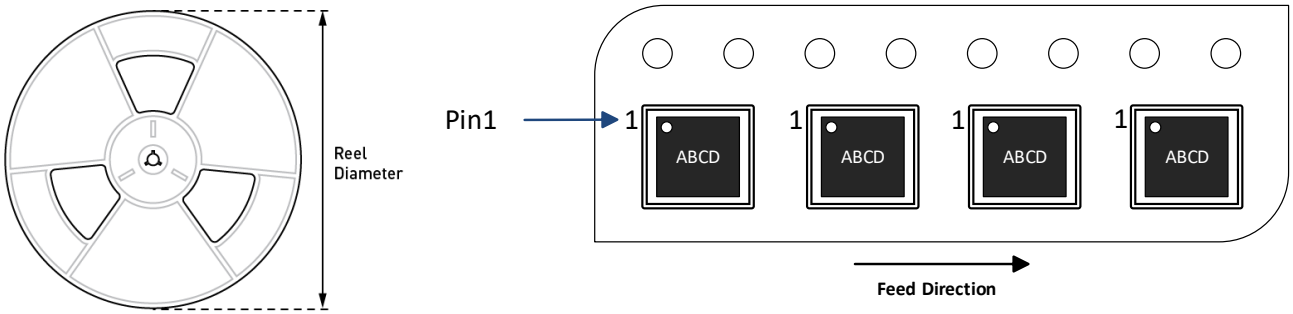


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6603GV-Z	QFN-25 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/24/2024	Initial Release	-
1.1	8/14/2025	Updated the ISET pin current ratio's Min/Max values in the Electrical Characteristics section to 10.81/12.19, respectively.	7